

CLAIMS

What is claimed is:

1. A non-volatile memory comprising:

2 a chalcogenide storage element;

3 a voltage limiting circuit, coupled to said chalcogenide storage element, for
4 ensuring that voltages across said chalcogenide storage element do not exceed a
5 predetermined value during a read operation;

6 a current-to-voltage converter circuit, coupled to said voltage limiting circuit,
7 for converting a current pulse read from said chalcogenide storage element to a
8 voltage pulse during said read operation; and

9 a buffer circuit, coupled to said current-to-voltage converter circuit, for
10 sensing said voltage pulse to determine a storage phase of said chalcogenide storage
11 element during said read operation.

1 2. The non-volatile memory of Claim 1, wherein said current-to-voltage converter
2 circuit includes a p-channel transistor, an n-channel transistor and an inverter.

1 3. The non-volatile memory of Claim 1, wherein said chalcogenide storage element is
2 capable of changing from an amorphous phase to a crystalline phase, or vice versa, via an
3 application of an appropriate amount of current.

1 4. The non-volatile memory of Claim 3, wherein current for said chalcogenide storage
2 element to reach said amorphous phase and said crystalline phase are 1 mA and 0.5 mA,
3 respectively.

1 5. The non-volatile memory of Claim 1, wherein said non-volatile memory further
2 includes a row decoder circuit for receiving an address input and a clock input.

1 6. A write circuit for writing data to a non-volatile memory, said write circuit
2 comprising:

3 a chalcogenide storage element;

4 a write control circuit for receiving a write_enable input, a col_write input
5 and a data_in input;

6 a row decoder circuit, coupled to said chalcogenide storage element, for
7 receiving an address input and a clock input; and

8 a write current supply circuit, coupled to said write control circuit and said
9 chalcogenide storage element, for writing data to said chalcogenide storage element
10 during a write operation under the control of said write control circuit.

1 7. The write circuit of Claim 6, wherein said write current supply circuit includes two
2 p-channel transistors.

1 8. The write circuit of Claim 6, wherein said chalcogenide storage element is capable
2 of changing from an amorphous phase to a crystalline phase, or vice versa, via an
3 application of an appropriate amount of current.

1 9. The write circuit of Claim 8, wherein current for said chalcogenide storage element
2 to reach said amorphous phase and said crystalline phase are 1 mA and 0.5 mA,
3 respectively.

1 10. A read circuit for reading data from a non-volatile memory, said read circuit
2 comprising:

3 a chalcogenide storage element;

8 a current-to-voltage circuit, coupled to said read control circuit and said
9 chalcogenide storage element, for sensing a current flowing through said
10 chalcogenide storage element during a read operation under the control of said read
11 control circuit.

1 11. The read circuit of Claim 10, wherein said current-to-voltage circuit includes a p-
2 channel transistor, an n-channel transistor and an inverter.

1 12. The read circuit of Claim 10, wherein said chalcogenide storage element is capable
2 of changing from an amorphous phase to a crystalline phase, or vice versa, via an
3 application of an appropriate amount of current.

1 13. The read circuit of Claim 12, wherein said flow-through current is 1 mA and 0.5
2 mA when said chalcogenide storage element is in said amorphous phase and said crystalline
3 phase, respectively.

1 14. The read circuit of Claim 10, wherein said read circuit further includes a buffer for
2 buffering output voltages from said current-to-voltage converter circuit.